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PCI EXPRESS™

PCI Express
Electrical Performance
Validation

Agenda

- PCI Express – Next Generation Performance
- PCI Express – What you should be testing
- PCI Express Compliance – What you will be judged against
- PCI Express Debug – What to do if you experience a compliance failure
- Summary

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What is covered in the presentation

Why PCI Express?

Productivity Personal Computer	Multimedia Personal Computer	Extended Personal Computer
mid 80's	Late 90's	2000+
386 processor 25MHz ISA Graphics Word Processing	Pentium® III processor 933MHz 3D Gaming Productivity Computing (ex. CAD)	2.5 +GHz Multimedia (Video & Audio) Video capture/edit PDA, MP3 Player, Camera Gigabit Ethernet, Wireless

New Usage Models Demand Greater I/O Bandwidth

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The development of PC Express was driven by the need for much greater performance. I/O performance needed to be improved to keep pace with processor and memory system performance.

PCI Express Overview & Benefits

A 3rd Generation I/O Interconnect

- **Scalable Performance**
  - **Multiple Connection Types**
- **Compatibility with PCI at the software layers leverages existing investment in software (PCI 2.3 compatible)**
- **Will co-exist along side PCI devices**
- **Advanced Features**
  - **Hot Plug and Hot Swap support enhances ease of use**
  - **Improved QoS ability via peer-2-peer communication that does not involve the processor.**
- **Low power consumption and power management functions offer greater reliability and high availability**
- **Support for next-generation 3D multi-media**
- **Allows for more flexible system architectures providing a potential cost savings.**

PCI Express Electrical Meas

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Here are some benefits of the technology. The biggest advantage is that it leverages the PCI software investment that a company has made in legacy PCI applications.
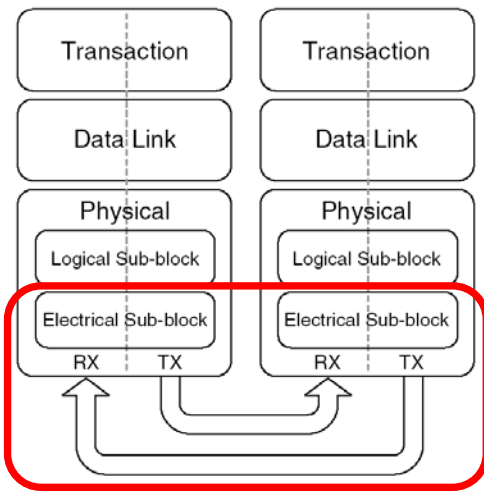
Agenda

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PCI Express Electrical Meas

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What is covered in the presentation

Electrical Testing Requirements Overview

Transaction	Transaction
Data Link	Data Link
Physical — Logical Sub-block	Physical — Logical Sub-block
Electrical Sub-block — RX	TX	Electrical Sub-block — RX	TX

This eSeminar covers the ACTIVE electrical testing requirements of the Physical Layer Electrical Sub-block.

- **PCI Express Base Specification, Chapter 4 (Transmitters and Receivers)**
- **PCI Express CEM Specifications, Section 4.7 (Add In Card Connector)**
- **PCI Express CEM Specification, Section 2.6.3 (Reference Clock)**

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Here is a high level picture of the PCI Express stack or architecture.

We will primarily look at the ACTIVE electrical measurements related tot he Electric Sub-Block.

By ACTIVE, I mean measurements with active 2.5 Gb signals.

For example, we will not be discussing characterization of backplane impedances.

More specifically (click), we will cover the specifications in chapter 4 of the base scec. These specs cover the transmitter and receiver silicon.

We will also talk about compliance measurements at the add in card connector, as defined in section 4.7 of the CEM spec.

And we will finish up by looking at the reference clock specs, as defined the CEM spec.

Overview of PCI Express: Electrical Signaling

Card Connector

PHY TX / RX

PHY RX / TX

Add In Adapter Card

100 MHz Reference Clock w/SSC

System (Motherboard)

- **2.5 Gbps Differential (1.25 GHz Fundamental)**
- **Embedded 8/10bit clocking**
- **Multiple Lanes Formats: X1, X4, X8, X16, X32**
- **Tr, Tf < 100 ps, 20~80%**
- **Spread Spectrum Clocking (SSC) using Reference Clock**
- **50 Ω termination for single-ended, 100Ω for differential**
- **De-emphasis bit - drop differential voltage level by 3.5±0.5 dB on non-transition bits.**

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PCI Express is a point to point, serial interconnect version of the popular PCI interface used in PCs. PCIE will provide additional performance while simplifying the layout of complex motherboards.

A PHY transmitter and receiver exists on both the motherboards and add in card.

Note that PCIE is not limited just to Add in cards, but can be used as a chip to chip interface on a circuit board, or as a system to system interface over a cable.

PCIE runs at 2.5 Gbs, and uses 8B/10B encoding, for a overall transfer rate of 250 MB/sec per lane.

Up to 32 lanes in each direction are supported.

The rise and fall times of PCIE are under 100 pS.

Spread Spectrum Clocking is implement via a 100 MHz reference clock..

The signals are source and load terminated to 50 ohms single ended, 100 ohms differential.

PCI Express uses a digital equalization method, which peaks transition bits 3.5 dB, as shown in the figure.

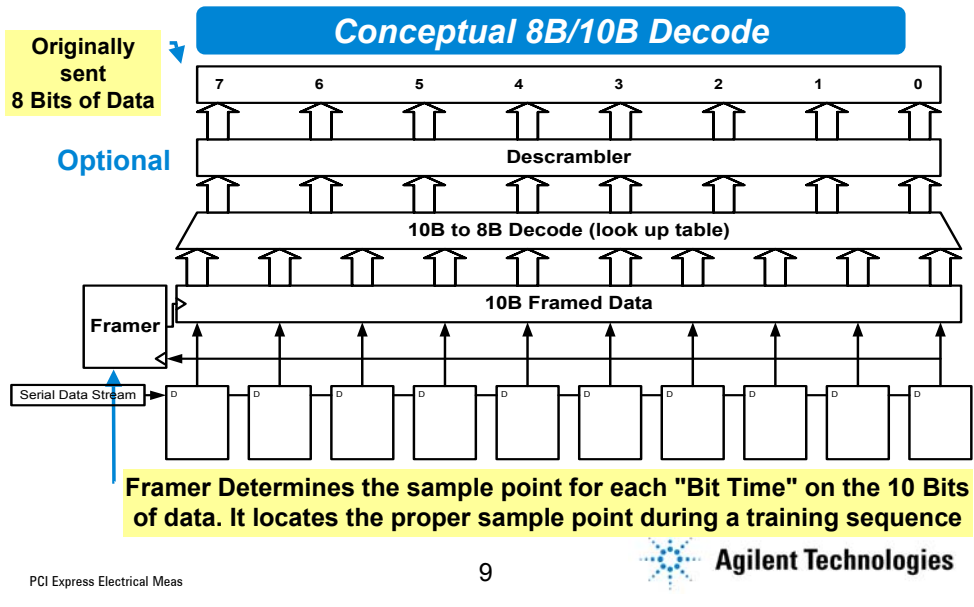# PCI Express Design & Debug Challenges:

Multi-lane Buses

Byte 1	
Byte 0	
Byte 7	
Byte 6	
Byte 5	
Byte 4	
Byte 3	
Byte 2	
Byte 1	
Byte 0	

Encoder Par -> Ser

Lane 0

Byte 1 / Byte 0 / Byte 7 / Byte 6 / Byte 5 / Byte 4 / Byte 3 / Byte 2 / Byte 1 / Byte 0

Byte 4 Byte 0	Byte 5 Byte 1	Byte 6 Byte 2	Byte 7 Byte 3
Encoder Par -> Ser	Encoder Par -> Ser	Encoder Par -> Ser	Encoder Par -> Ser
Lane 0	Lane 0	Lane 0	Lane 0
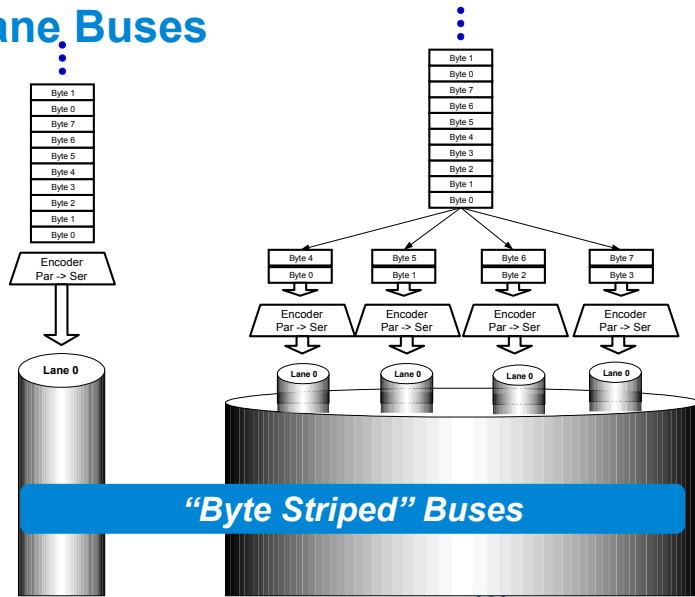
"Byte Striped" Buses

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Multi-lane byte striped "busses" require that data on each lane be reconstructed to show true data flow but again make debug much more difficult compared to conventionaly parallel bus structures.

PCI Express Design & Debug Challenges:

8B/10B Encode/Decode

Conceptual 8B/10B Decode

Originally sent 8 Bits of Data

7	6	5	4	3	2	1	0

Optional

Descrambler

10B to 8B Decode (look up table)

10B Framed Data

Framer

Serial Data Stream

Framer Determines the sample point for each "Bit Time" on the 10 Bits of data. It locates the proper sample point during a training sequence

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8B/10B and optional bit scrambling can help reduce EMI problems but can also make the interconnect harder to debug logically.

PCI Express Design & Debug Challenges:

Chip-to-Chip and Microwave bus speeds

1 Lane = 2 Differential Pairs (1 send, 1 receive)

Device A

Device B
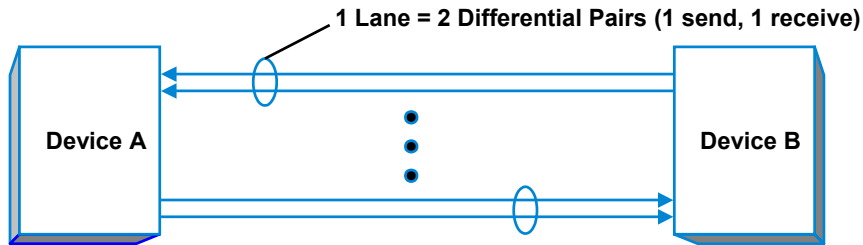
- **Dual Simplex Point-to-Point Topology**
- **LVDS (Low Voltage Differential Signaling) Technology**
- **$\geq$ 2.5 Gb/s per Lane/direction**
- **Selectable Lane Width**
  - **x1, x4, x8, x16, x32**

Problem Areas:
- **Crosstalk**
- **Impedance Discontinuities**
- **Reflections**
- **InterSymbol Interference**
- **Mode Conversion**

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PCI Express using high speed, 2.5Gbit/s serial links can suffer from a large array of physical phenomena including crosstalk, impedance discontinuities resulting in reflections (causing jitter), intersymbol interference, and mode conversion due to unbalanced transmission lines can lead to excessive EMI emissions in a large system.

PCI Express Physical Layer Characterization
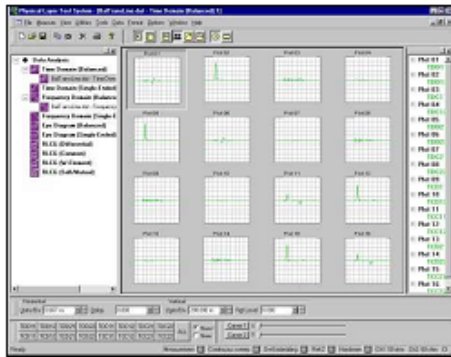
Physical Layer Test System (PLTS)

- **Complete characterization of your device with one tool**
- **Works with both a VNA or TDR scope**
- **Unparalleled accuracy delivers confidence in measurements**
- **Superb for creating models for simulations**
- **Save time by Measuring multiple parameters with 1 setup**
  - **Insertion Loss (SDD21)**
  - **Return Loss**
  - **Mode Conversion (SCD11, SCD21)**
  - **Differential Trace Impedance (SDD11)**
  - **Data dependent jitter**
- **Also can measure Crosstalk (FEXT, NEXT)**

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The PLTS Software tool can be used with a TDR or VNA to provide the highest level of accuracy when characterizing or modeling transmission lines in a PCB, Cable, or connector.

Device Characterization: Transmitters

Measurements performed with an Equivalent Time Oscilloscope

Measurements	86100C DCA-J Sampling Oscilloscope w/TDR & PLTS
Rise time, Fall time, Impedance, Return Loss *	✓

- **Can also use a VNA for Return Loss Measurements.**
- **Could measure UI time, Voltages, Eye Mask, Idle timing, Land Skew w/clock recovery**

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To fully characterize a PCI Express Transmitter, both an real time and sampling scope in needed.

The table lists all the measurements needed, based upon the PCI Express specification.

Most specification are required to be measured over 250 consecutive UI (unit intervals), and therefore require a real time scope with serial data analysis capability. A sampling scope does not measure consecutive UIs.

However, the risetime specification is too fast for real time scopes available today, so a sampling scope must be used.

Also, the sampling scope provides TDR capability which is used tom measure the impedance.

The return loss can be measured with a TDR and PLTS software, or alternatively, a VNA can be used.

For the most accurate measurements, a direct connection from the transmitter's TX output to the scope inputs should be used. This offer the lowest noise measurement.

If a direct connection is not possible, then a differential prove proves good performance also, but adds a small amount of noise and jitter to the measurement.

In the case of the risetime, impedance, and return loss measurements, a direction connection is required.

Device Characterization: Transmitters

Measurements performed with a Real Time Oscilloscope

Measurements	54855A 6 GHz Real Time Oscilloscope w/E2688A SDA
UI time, Voltages, Eye Mask, Jitter, Idle Timing, Lane Skew	✓

PHY Transmitter TX+ TX-
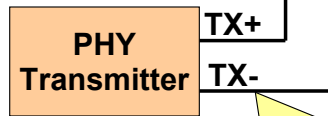
A direct connection provides best performance; and is required for measurement of rise time, impedance, and return loss. A probe connection is good when a direct connection is not possible.

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In the case of the risetime, impedance, and return loss measurements, a direction connection is required.

Here is an example of a eye and jitter measurement on a transmitter transition bit.

Notice on the eyes after a transition bit are being measured.

The color graded display give statistical information on the signals noise and jitter.

The eye mask and jitter measurement are made over 250 consecutive UIs.

Multiple acquisitions can be made to find worst case eye and jitter over multiple sets of 250 consecutive UIs.

Mask test failures can be logged, and used to generate email notifications.

The jitter histogram can be displayed for diagnostic information.

The E2688A uses the SigTest DLL for consistent measurement results with compliance testing performed using SigTest. More on this in upcoming slides.

Device Characterization: Receivers

A signal generator is used to stimulate the receiver, and the response of device is monitored*

Stimulus:

Training Sequence TS1
....0011011100...

RX

PCI Express
DUT

TX

Response:

Training Sequence TS2
....0011011100...
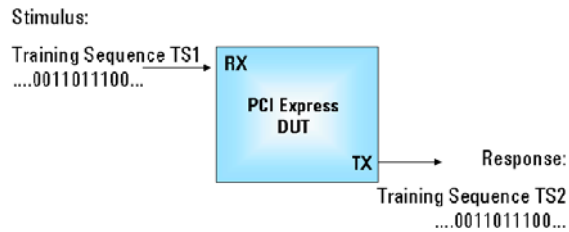
- **Most testing can be performed with an 81134A Pulse Pattern Generator and a function generator as the stimulus source.**
- **An oscilloscope & probe is used to monitor the signal into the receiver.**
- **An oscilloscope or logic analyzer is used to monitor the response from the device.**
- **Receiver input impedance and return loss is measured with a TDR or VNA.**

More Info: Agilent Product Note 5988-7432EN

* Assumption:
The response is correct if
1) the RX input received the stimulus signal correctly and
2) the subsequent stages of the DUT processed it properly.
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Receivers must be tested for the sensitivity, and tolerance to jitter.

The testing methodology is to provide a stimulus to the RX input of a device, and monitor the response from the device via the TX pins. Note that this testing methodology assumes that the device's is functional enough to response correctly to Training Set inputs on it's RX inputs.

An signal generator such as the Agilent 81134A is ideally suited for most tests, the exception being lane to lane skew tests.

A function generator is used to add jitter to the stimulus signal.

The signal should be monitored at the device's input pins with an oscilloscope and probe, to know what the actual signal amplitude and jitter is AT the device's input.

The response from the device can be monitored with an oscilloscope or logic analyzer.

In additional to sensitivity and jitter tolerance, the receiver's input impedance and return loss must be measured with a TDR or VNA.

For more receiver testing, Agilent has a detailed product note, part number 5988-7432EN. This product note can be found by typing the part number in the search window at www.agilent.com.

PCI Express Compliance Checklists

Electrical Sub-Block

Component meets assertion?

PHY.3.1#1	The bit rate clock source for transmitter and receiver must be +/- 300 ppm or better.	yes ____ no ____
PHY.3.1#2	If SSC is used, the data rate must be down-spread and modulated no more than 0.5% of the nominal data rate frequency.	yes ____ no ____
PHY.3.1#3	If SSC is used, the modulation rate must not exceed the range of 30 kHz - 33Khz.	yes ____ no ____

. . .

Vendors are expected to complete ALL compliance checklist measurements for their device.

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What is covered in the presentation

Compliance = Interoperability = Market Adoption

- **PCI-SIG & Intel collaborate for compliance testing**
  - **Intel developed compliance utility: SigTest**
  - **Intel developed compliance fixtures:**
    - **Compliance Load Board (CLB), Compliance Base Board (CBB)**
  - **Testing is not comprehensive (audit only)**

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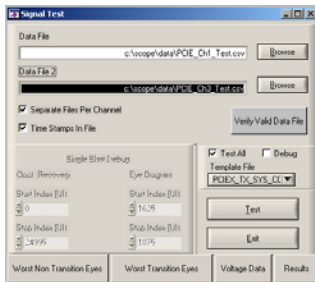
Compliance is necessary to ensure products are interoperable. Nobody wants to buy a hot new graphics card from ATI only to find out that it doesn't work in their Intel motherboard.

What's a Plugfest?

- **PCI Express Logo Program**
  - **Vendors must validate system platforms and add-in cards to make "Integrator's List"**
- **PCI-SIG (Special Interest Group) Governing Body**
  - **Drive Specification Development**
  - **Authorization/Enforcement of Logo Usage**
  - **Organize and Conduct Plugfests**
- **Interoperability is the Main Goal**
- **Plugfest Events Occur quarterly in Milpitas, CA and sometimes elsewhere (Taiwan, …)**
- **Testing requires a 6 GHz, 20 GSa/s real time scope (Agilent 54855A), fixture boards, and SigTest measurement application.**

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Plugfests are crucial to ensuring interoperability. Here vendors qualify their products for consistency with the PCI Express standard.

Compliance Test Setup for Add-in Card
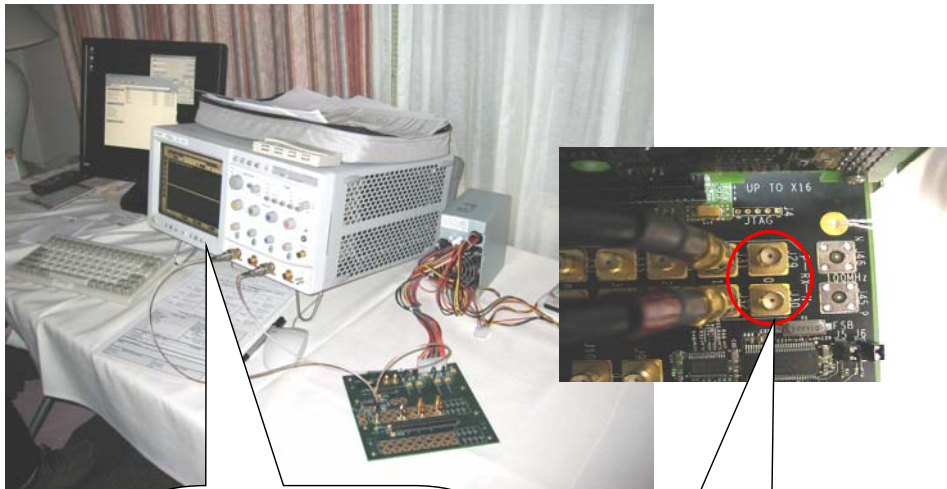
Vendor Neutral Setup – Chan 1 & 3, 6 GHz inputs

Pos & Neg SMA Measurements

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The PCI Express compliance tests are structured around the real-time oscilloscope. An Intel designed compliance test fixture is used to connect the DUT to the instrument. Two fixtures are used in testing depending on the DUT. For motherboards, a Compliance Load Board (or CLB) is used. For add-in cards a Compliance Base Board (shown) or CBB is used.

PCI Express Compliance Test Pattern
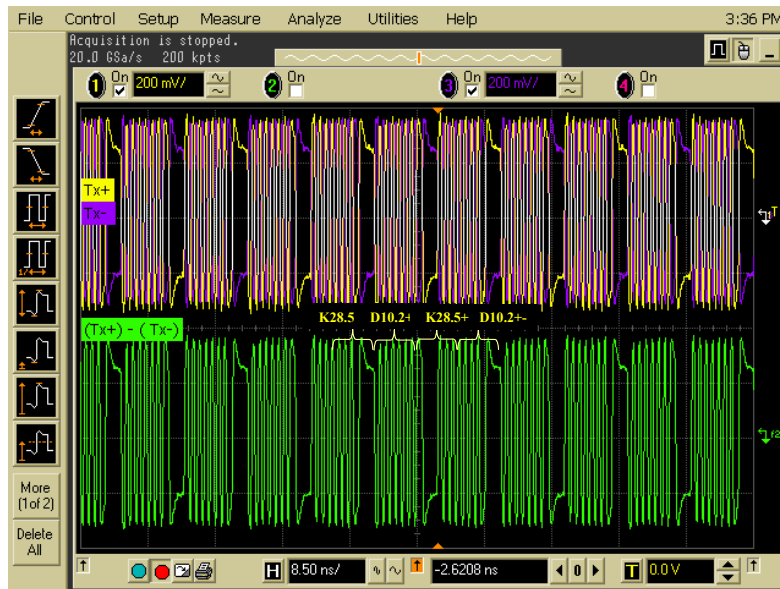
When a DUT is placed in the CLB or CBB it will emit a compliance test pattern shown here. This is a pattern specified in the PCI Express standard that stresses the interconnect much as actual traffic would. This is used to show signal quality.

SigTest Compliance Analysis
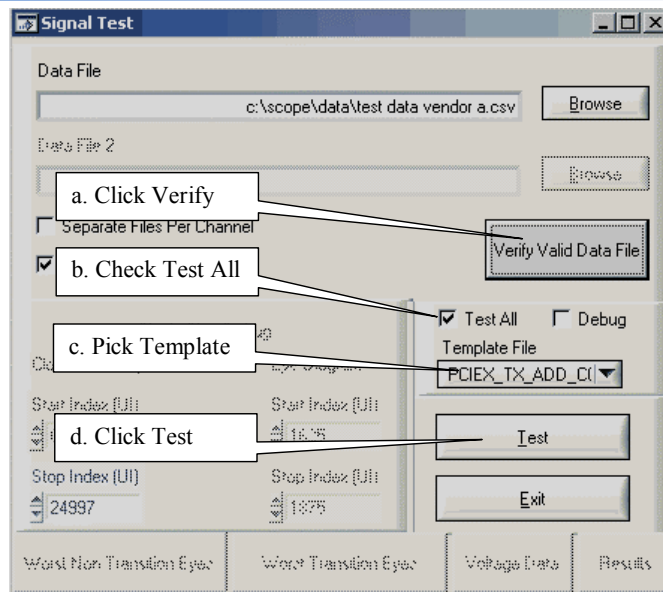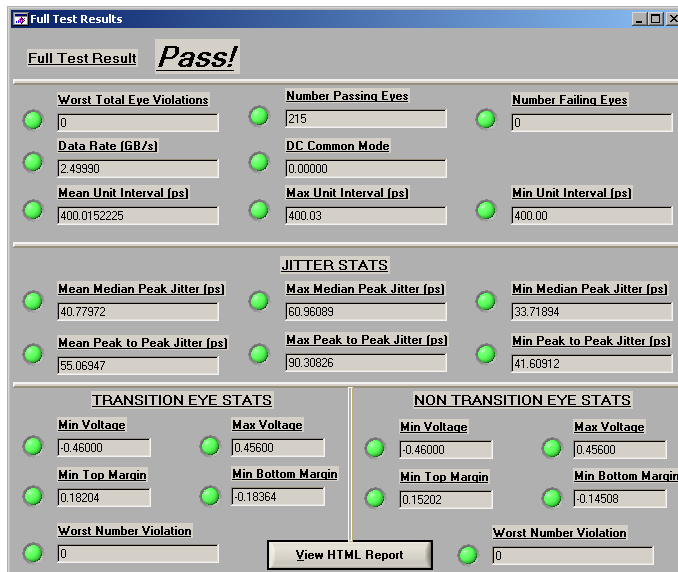
The PCI Sig has issued a signal quality test utility program called SigTest. This program is used to validate that a particular DUT is compliant with the PCI Express specification. The Oscilloscope captures the waveform (shown in the previous slide) and it is loaded into the SigTest utility. SigTest then generates a compliance summary and report.

The PCI Sig has issued a signal quality test utility program called SigTest. This program is used to validate that a particular DUT is compliant with the PCI Express specification. The Oscilloscope captures the waveform (shown in the previous slide) and it is loaded into the SigTest utility. SigTest then generates a compliance summary and report.

SigTest Report of Results

Test Results for PCIE_Ch1_Test

Worst Non Transition Signal Eye

Required Tests:

- **Overall Result: Pass!**
- **Data Rate: 2.499793 GB/s**
  Data Rate Pass!
- **Median to Peak Jitter: 63.256895 ps**
  Median to Peak Jitter Pass!
- **Peak to Peak Jitter: 92.178598 ps**
  Peak to Peak Jitter Pass!
- **Eye Violations: 0 points**
  Eye Test Pass!

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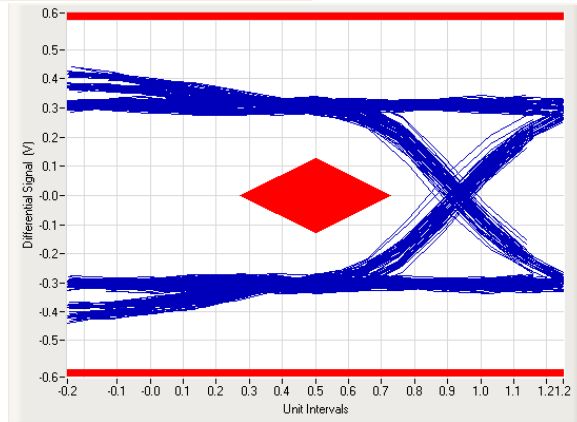
This is a sample SigTest report. There is limited amount of measurement and debug information – there are only 3 graphic images.

Agilent N5393A PCI Express Compliance & Validation Tool Suite

- **Key Features:**
  - Test setup wizard for ease-of-use
  - Wide range of electrical tests
  - Automated scope measurement setup
  - Test results report generation
  - Pass/fail margin analysis

- **Key Benefits:**
  - Saves time on complex tests
  - Easy UI
  - Good debug and analysis tool
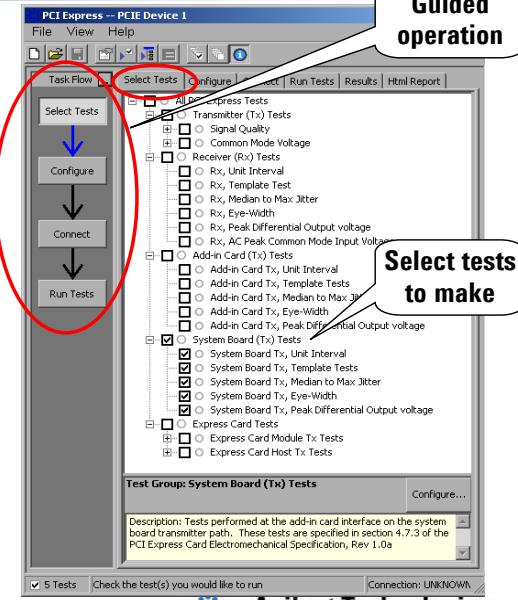
PCI Express Electrical Meas

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Keep in mind that SigTest covers only a subset of the physical layer tests required by the spec. It should be considered an audit verification. Vendors are still required to do all of the tests called for in the PCI Express specification. The Agilent N5393A Compliance and validation test suite is a structured, automated measurement application that performs many more tests than SigTest. Used in conjunction with the E2688A Serial Data Analysis application, the N5393A forms a powerful debug tool for identifying and fixing compliance failures.

The software is very easy to use. You start by defining which tests you want to make. When you click on a measurement, a short description appears in the bottom window.
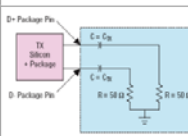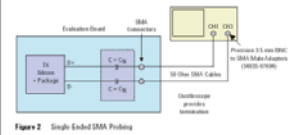
Test Setup Configuration

The next step is to configure the test setup. Here you can add information about the test device, define how it is connected to the scope, etc. to guide the software.

Guided Setup Connections

The next step is making the test connections. Illustrations and/or photos are used to show how to hook things up. If the tests selected require a test setup change, you will be prompted later to make them. In this example, we only have to make a single connection for our tests. The software will automatically configure the scope for each measurement, make the the measurement, and save the results.

Run Tests and Show Results

Measured value

Margin warnings indicate yield issues

Pass/Fail status

Individual Test will be documented here

When the measurements are complete, the N5393A provides a measurement summary on screen. In addition to pass/fail status and the actual measured values, a marginal analysis to show you just how close you are passing a given spec. This is important to help you to show how much margin is in your system and where your system is most sensitive.

HTML Report Test Summary

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| Report Style |
| Compact *Verbose* |

PCI Express Test Report

Overall Result: **FAIL** (1 of 16 Tests Failed)

Test Configuration Details	
User Comments	
Device Type	
Device ID	Device 1
Number of Lanes	
Last Test Date	5/28/2004 2:16:37 PM
Model Number	54855A
Serial Number	No Serial
Infiniium SW Version	03.49.5002R

DUT documentation

Margin warning thresholds

Summary of Results

Margin Thresholds	
Warning	<= 15 %
Critical	<= 0 %

Measured value

Pass/ Fail status

Pass	Test Name	Spec Range	Measured Value	Margin
✓	System Board Tx, Unit Interval	[399.88ps to 400.12ps]	399.97ps	37.1 %
✓	System Board Tx, Template Tests	Zero Mask Failures	0	N/A
✓	System Board Tx, Median to Max Jitter	<= 108.50ps	52.50ps	51.6 %
✓	System Board Tx, Eye-Width	>= 183.00ps	315.01ps	72.1 %
✓	System Board Tx, Peak Differential Output voltage	[0.2530V to 1.2000V]	0.9200V	29.6 %
✓	Tx, Unit Interval	[399.88ps to 400.12ps]	400.05ps	29.6 %
✓	Tx, Template Tests	Zero Mask Failures	0	N/A
✓	Tx, Median to Max Jitter	<= 60.00ps	48.80ps	18.7 %
✓	Tx, Eye-Width	>= 0.700UI	0.794UI	13.4 %
✓	Tx, Peak Differential Output voltage	[0.8000V to 1.2000V]	0.9372V	34.3 %
✓	Tx, Rise/Falltime	>= 50.00ps	205.47ps	310.9 %
✗	Tx, Deemphasized Voltage Ratio	[-4.0dB to -3.0dB]	-2.7dB	-20.8 %
✓	Tx, RMS AC Peak Common Mode Output Voltage	<= 20.0mV	16.1mV	19.5 %

Margin warnings

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For more extensive measurement results, an HTML report format is available. Here you get documentation on the DUT and test setup, your margin thresholds, and the results. Like the on screen display, pass/fail status, actual measure values, and margin are displayed.

HTML Report Test Description and Analysis

If we scroll down the HTML report, for each measurement a complete summary is displayed. Here we see a description of the test, the summary of measurements, and display snapshots when appropriate. This is very helpful for analyzing your device. Finally, you can save this test as a project file so that it can be re-run in the future and/or the test results saved for later review.

Reference Clock

- **The system board provides a 100 MHz reference for transmitter and receiver synchronization and SSC tracking**
  - **The reference clock specifications can be measured with an Agilent 54855A scope and two 1134A InfiniiMax probes.**
  - **Jitter analysis software is required to measure the clock jitter and SSC profile.**
  - **The 1 Meg memory option is also required to measure the SSC profile.**

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System boards provide a 100 MHz reference clock to all transmitters and receivers.

The transmitters generate their TX clock from this reference.

The receivers may use the ref clock, depending on the receiver architecture used.

Spread Spectrum may be applied to the reference clock, at a rate of 0.5% at 33 kHz. This will propagate to the TX clocks in the transmitters. Some reciever architectures will need to use the refclock to adequately track the SSC.

The reference clock can be measured with an Agilent 6 GHz real time scope and two probe.

Two probes are required because the specifications call out some single ended specs.

A jitter analysis option is needed to make the jitter measurement, and to perform an measurements of the SSC profile. Either the E2681 or E2690 will suffice for this.

For SSC measurements, the 1 Meg memory options is needed to capture at least one cycle of the SSC.

Reference Clock (cont)

Example of Reference Clock Measurement
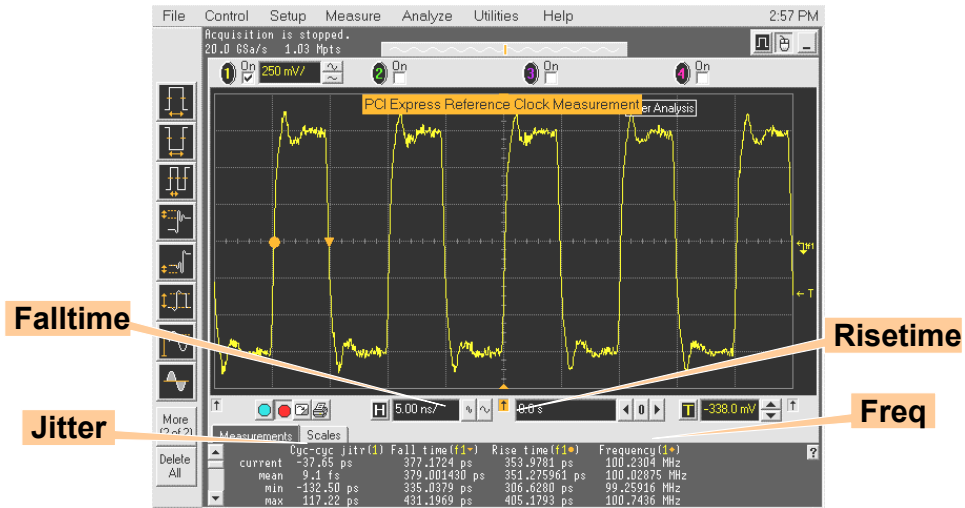
Here is a measurement of a ref clock using the 54855A.

In this example, we see measurement of the cycle-cycle jitter, risetime, falltime, and frequency.

In this example, we used the E2681A for the jitter measurement.

This measurement is being made as per the current specification for the refclock, which is a cycle-cycle spec.

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What is covered in the presentation

Tools For Debug

What do you do if a compliance test Fails?
What do you do if you want to test more than just compliance?

E2688A High Speed Serial Data Analysis Wizard
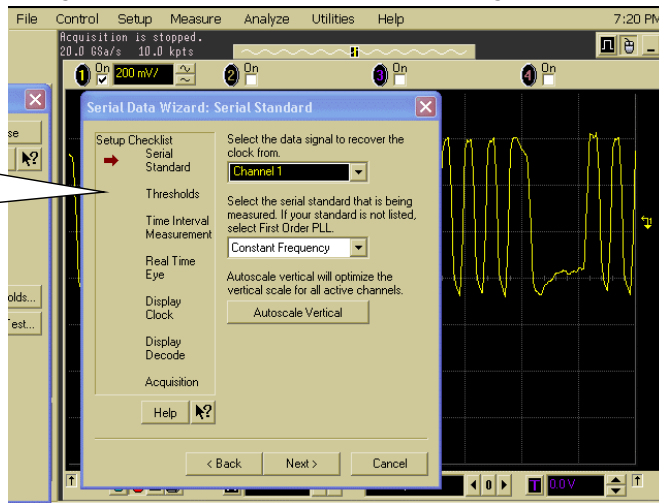
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New enhancements to the E2688A Serial Data Analysis application include serial decode, serial triggering, and eye-mask unfolding. These capabilities are crucial to assist in the debugging of compliance failures due to signal integrity problems.

Serial Decode of a PCI Express Signal (setup)
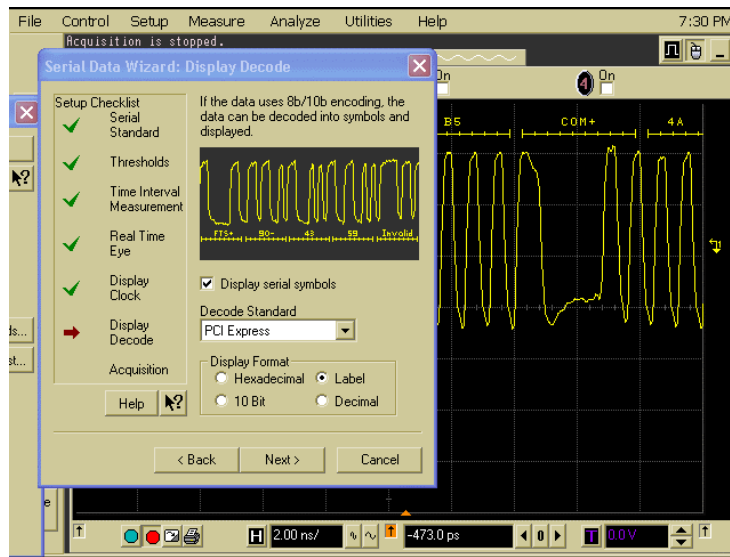
Here you can see the setup for serial decode of the PCI Express signal. The breakthrough discovered here is that each standard has a specific sequence of 0's and 1's that are unique. Once we locate this alignment character we are able to decode the entire trace into multiple formats. Supported standards for decode include PCI Express, Fibre-Channel, SATA, and InfiniBand. A custom decode option for proprietary standards is also provided.
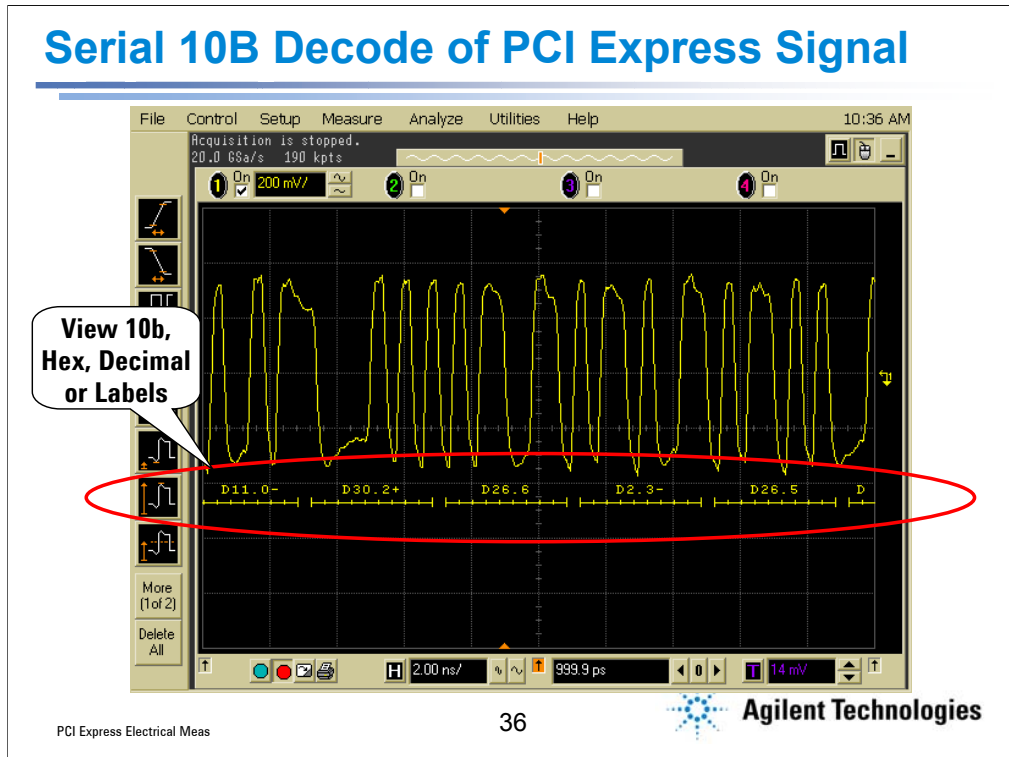
This slide shows the 10B codes of the PCI Express signal. We can also display standard specific labels or show the bits in decimal or hex formats.

Search and Trigger

In looking at the PTC pattern, what if our system has a problem and we see an invalid character – something that isn't a pre-defined symbol. Before the software engineers can validate their protocol, the electrical engineer will need to make sure they aren't sending bad symbols. If we click on the 8b/10b decode Setup button, we can define a search criteria of up to 4 symbols. Since 8b/10b is generic, every standard has a different symbol map. We can see on the right hand side that there are unique control codes. You can consider these to be punctuation. For PCI Express, the COM character is a comma. You select a different standard like Fibre Channel to see the differences. There is a User Defined mode where you can edit a text file on the scope to define your own symbol map, so the tool is very flexible.

Let's envision that after the COM and B5 symbols, we periodically get an invalid symbol. We can select COM, then B5 and enable the Trigger on Search and/or Stop on Trigger to look for this symbol sequence in our data stream.

After enabling the search, you'll find some navigation controls on the lower portion of the display. We can scroll through all instances of the search string to see if we find any invalid characters. This is a very powerful debug capability and it's unique to Agilent's scopes.
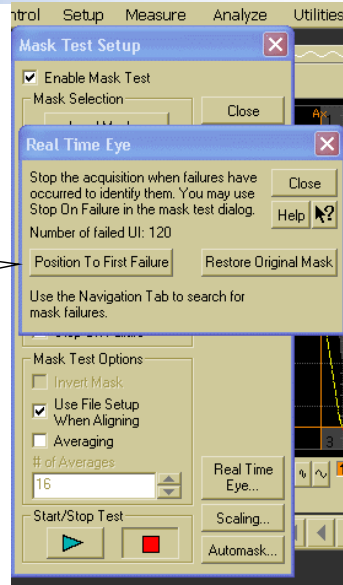
Locating Eye Mask Violations

The real-time eye combined with the eye mask test indicates there were multiple violations. But how do you gain insight into the individual violations by looking at the composite eye?

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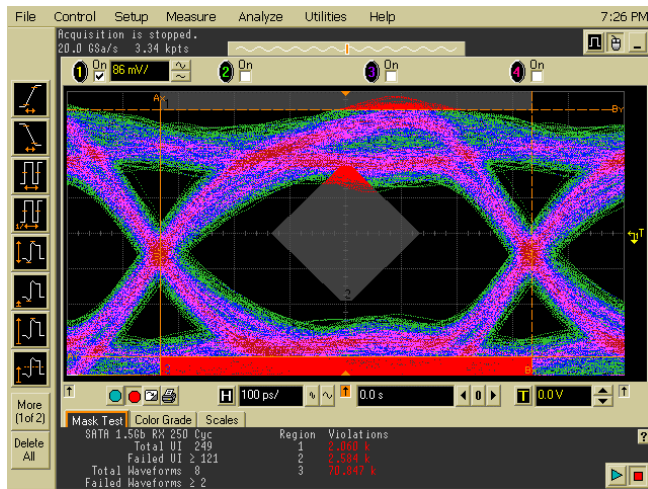
Another big debug feature is the Eye Mask Unfolding. When we perform an eye mask test, if we have failures a portion of the eye mask screen is highlighted in red. Since this is a real-time eye display, it's a compilation of all the transitions in our data stream. It's impossible to determine which ones caused the failure.

Locating Eye Mask Violations

Using the controls in the HS-SDA, we can instruct the scope to go to the first violation in the serial data stream.

If we go to the eye mask menu, we'll see this new selection to go to the first mask failure.

Locating Eye Mask Violations

Mask Failure

Number of instances

Navigate to all the instances of the eye mask violation using the arrow keys

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Like the symbol search, the eye mask unfold will let us scroll through all the sequences in our data stream that failed the eye mask test. Now we can see that the failed waveform, in this case the signal failed the maximum voltage test and we have a better understanding of what we will need to fix.

Agenda

PCI EXPRESS™

- PCI Express – Next Generation Performance
- PCI Express – What you should be testing
- PCI Express Compliance – What you will be judged against
- PCI Express Debug – What to do if you experience a compliance failure
- Summary

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What is covered in the presentation

PCI Express Electrical Layer Validation

- **Transmission Line Characterization**
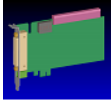- **Device Transmitter/Receiver Characterization**
- **Compliance Testing**
- **Debug**

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Agilent PCI Express Electrical Validation Tools

- **54855A 6-7 GHz 20 GSa/Ch, 4 channel Oscilloscope**
  - E2690A Time Interval & Jitter Analysis software
  - E2681A EZJIT Jitter Analysis software
  - E2688A Serial Data Analysis software with 8b/10b decoder
  - N5393A PCI Express Compliance Test software
  - 1134A InfiniiMax 7 GHz Active Differential probe
- **86100C Digital Communications Analyzer w/ TDR plug-in**
- **81134A 3.35 GHz 2 Ch. Pulse Pattern Generator**
- **N1930A PLTS (Physical Layer Test System) software for VNA and TDR**

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Agilent PCI Express Tools

E2960 Exerciser/Analyzer
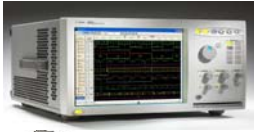
E2969A PCI Express Protocol Test Card

16900 Logic Analyzer

N1930A Physical Layer Test System (VNA or TDR)

86100C DCA-J with TDR

N4220B Packet Analysis Probe

81134A Pulse Generator

N4901 Serial BERT 81250 ParBERT

54855A Infiniium Oscilloscope

Config./OS

Software

Transaction

Data Link

Physical

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PCI Express Electrical Meas

45

Agilent is ready now with solutions to address problems across the entire spectrum of the PCI express application space. From physical layer testing to application testing.

Agilent Technologies:

A Core Player in the PCI Express World

- **Key contributor in the PCI-SIG**
- **Heavily involved in compliance and interoperability tests (since PCI intro)**
- **Agilent, Intel and Xilinx demo the world's first PCI Express system in IDF-Spring, Feb. 2004**
- **Agilent 54855A Infiniium Oscilloscope adopted at IDF 2003 San Jose due to it's superior accuracy and probing system**
- **Jointly developed and announced with Intel Corp the E2969A PCI Express Protocol Test Card at the PCI SIG Developers Conference in June 2003**
- **Introduced the world's first PCI Express Exerciser/Analyzer (E2960) at the PCI SIG Developers Conference in June 2003**

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Agilent has been and continues to be a strong force in support of PCI and PCI Express. Agilent has forged a very close relationship with the PCI-Sig and Intel to offer leading solutions for PCI Express developers.

Resources

- **PCI Express Products & Application Info**
  www.agilent.com/find/pci_express
- **Signal Integrity Application Info**
  www.agilent.com/find/si
- **Jitter Application Info**
  www.agilent.com/find/jitter_info
- **PCI SIG**
  www.pcisig.com

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Agilent's list of application information is continually growing. See the web site on this slide for the lastest information on application notes, design guides, and solution information for PCI Express deployment.